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REMARKS

In the Office Action, the Examiner noted that claims 1-50 are pending in the application and that claims 1-50 are rejected. By this response, claims 7 and 9-10 are amended. In view of the following discussion, Applicants submit that none of the claims now pending in the application are indefinite under the provisions of 35 U.S.C. §112 or obvious under the provisions of 35 U.S.C. §103. Thus, Applicants believe that all of these claims are now in condition for allowance.

CLAIM INTERPRETATION

The Examiner provided an interpretation of and invited clarification for "directly accessing" as recited in claim 1; and "data-in pointer logic" and "data-in latch logic" as recited in claim 39. Applicants' arguments set forth below do not rely on the interpretation of these terms. Applicants neither accept nor reject the Examiner's interpretation of these terms, but rather consider the issue moot in view of the following arguments.

CLAIM OBJECTIONS

The Examiner objected to claim 9, stating that the connection to the first trigger input is unclear. The Examiner also stated that the connection to the third logic input is unclear. (Office Action, p. 3). First, claim 9 depends from claim 8, which states that "the second logic updates to the first vale of the first data and presents the first data to the second input of the first logic when a trigger signal is received at the first trigger input." (Emphasis added). That is, the first trigger input receives a trigger signal. Thus the connection to the first trigger input is clear. Second, Applicants have amended claim 9 to clarify that the third logic input is configured to receive the new value of the first data tat is stored in the third logic. Thus, the connection to the third logic input is clear. Accordingly, Applicants respectfully request that the objection to claim 9 be withdrawn.

REJECTIONS UNDER 35 U.S.C. §112

The Examiner rejected claims 7-9 and 10-18 under 35 U.S.C. §112, second paragraph. Applicants traverse the rejection.

The Examiner rejected claims 7-9 as having an insufficient antecedent basis for the term "timing logic associated with at least one latch." The Examiner rejected claims 10-18 as having an insufficient antecedent basis for the term "timing logic associated with at least one flip-flop." The Examiner stated that claim 1 does not recite timing logic, a latch, or a flip-

flop. (Office Action, pp. 3-4). Applicants note that a definite article (e.g., the or said) does not precede the term "timing logic", the term "at least one latch", or the term "at least one flip-flop" in claims 7 and 10. Thus, these terms signify new elements with respect to the elements of claim 1. No antecedent basis is therefore required for these terms in claims 7 and 10. To be consistent with subsequent dependent claims, Applicants have amended claims 7 and 10 to recite "a timing logic". Applicants respectfully submit that claims 7 and 10, as well as dependent claims 8-9 and 11-18, comply with 35 U.S.C. 112, second paragraph.

REJECTIONS UNDER 35 U.S.C. §103

The Examiner rejected claims 1-6, 19-36, 38, and 44-46 under 35 U.S.C. 103(a) as being unpatentable over Bhandari et al. (U.S. Patent No. 5,663,900 issued September 2, 1997) ("Bhandari") in view of Klein (U.S. Patent No. 5,771,370 issued June 23, 1998) ("Klein"); claims 7 and 10 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein and further in view of "Q-Modules: Internally Clocked Delay-Insensitive Modules" by Rosenberger et al. (IEEE Transactions on Computers, vol. 37, No. 9, Sep. 1988, pp. 1005-1018) ("RO'1998"); claims 8-9 and 11-18 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of RO'1998, further in view of "High Speed External Asynchronous/Internally Clocked Systems" by W.S. VanScheik et al. (IEEE Transactions on Computers, vol. 46, No. 7, Jul. 1997, pp. 824-829) ("VA'1997"); claim 37 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of Butts et al. (U.S. Patent No. 5,661,662 issued August 26, 1997) ("Butts"); and claims 39-43 and 47-50 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of "A Heterogeneous Environment for Hardware/Software Cosimulation" by William D. Bishop et al. (IEEE Transactions on Computers, 1997, pp. 14-22) ("BI'1997"). Applicants traverse the rejections.

A. Claims 1-6, 19-36, 38, and 44-46

The Examiner rejected claims 1-6, 19-36, 38, and 44-46 under 35 U.S.C. 103(a) as being unpatentable over Bhandari in view of Klein. (Office Action, p. 6). Applicants traverse the rejection.

Bhandari teaches an electronic simulation and emulation system for simulating or emulating a functional specification of a prototype design. (See Bhandari, Abstract). In particular, Bhandari teaches a software simulator having various simulation models that define the prototype design. Interface software and hardware are provided between the

software simulator and external systems. (Bhandari, col. 3, lines 6-29). The external systems may include a functional tester, logic analyzer, emulator, modeler, etc. The external systems cooperate functionally with, or monitor signals from, the software simulator by transferring data signals therebetween. (Bhandari, col. 3, lines 55-60). The Examiner has acknowledged, however, that Bhandari does not explicitly disclose a "shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." (Office Action, p. 7).

Despite the lack of explicit disclosure, the Examiner stated that Bhandari discloses that the second information comprises at least one internal state of the hardware model as such information would be vital to any hardware-software co-simulation system. (Office Action, p. 7). The Examiner has taken official notice that second information comprising at least one internal state of the hardware model would be vital to any hardware-software co-simulation system. It appears that the Examiner is arguing that Bhandari inherently teaches the aforementioned feature. Applicants address this issue immediately below before preceding to address the rejection of claims for obviousness.

First, Applicants traverse the Examiner's official notice. It is not common knowledge well-known in the art that information comprising at least one internal state of the hardware model is vital to any hardware-software co-simulation system. In support of the official notice, the Examiner cited U.S. patent 6,052,524, col. 14, lines 21-37, which states:

> Co-verification simulators known in art typically determine the internal behavior and state of hardware and software components every cycle of a simulator. This provides accuracy, but may slow the simulation by an order of magnitude or more. Cycle-accurate simulator 12 in a preferred embodiment of the present invention allows events to be set and the internal behavior and state of hardware components to be accurately examined at specific events (e.g., after a memory access). This allows cycle-accurate simulator 12 to provide faster simulations of hardware and software components. Cycle-accurate simulate 12 can also determine internal behavior and state of hardware and software components every cycle by setting a first event to occur on a first simulator cycle and a second event to occur on a second simulator cycle, a third event to occur on a third simulator cycle, etc.

Nothing in the cited passage, however, indicates that information comprising at least one internal state of the hardware model is "vital" to a co-simulation system. The passage states that co-verification systems "typically" determine internal behavior and state of hardware and software components. "Typically" does not mean vital or necessary, but rather indicates that in some cases co-verification systems do not determine internal behavior and state of

hardware and software components. Moreover, "determining" internal behavior and state of hardware and software components does not teach or suggest storing them in a shared memory, as recited in Applicants' claim 1.

The Examiner also cited the Abstract of U.S. patent 5,546,562, which states:

> An emulation modeling apparatus (54) comprises a combination of a device under simulation (48) to be emulated and means for keeping the device under simulation (48) in a quiescent state at normal operating speeds and in a normal operating sequence so as to allow dual access to the emulation modeling apparatus (54) without loss of data or accuracy of functions. One access is from a host simulation environment (26) while the other is from a model debug user interface (20) where internal architecturally visible registers and status are available to the user for greater debug control on the simulated subsystem within simulation environment (26). Specifically, any of a wide variety of physical VLSI circuits (48) to be modeled is kept in a quiescent state after power-on by a device control (50). It is then accessed through simulation means by simulated subsystem within a simulation environment (26), to change the architecturally visible internal state of the VLSI circuit (48). Control (50) brings VLSI circuit (48) out of the quiescent state and submits the requested simulated access. After taking the response, control (50) returns VLSI circuit (48) again to its quiescent state so as to keep its internal state current. The response is sent back to simulation environment (26) to update the simulated subsystem. Independently, any user request for accessing the architecturally visible internal state of the circuit is gathered by model debug and user interface (20). Interface (20) enables control (50) to bring VLSI circuit (48) out of the quiescent state and to submit the user request access. Subsequently, control (50) monitors the response and returns VLSI circuit (48) to its quiescent state so as to maintain the internal state of VLSI circuit (48) current. Control (50) then sends the response back to user interface (20). VLSI circuit (48) thus is always kept ready and current for the next request, either from simulation environment (26) or from user interface (20) without having to reset it. If any user defined breakpoint condition is met during the simulated accesses on the VLSI circuit (48), this information is forwarded by control (50) to simulation environment (26) for stopping the simulation and to user interface (20) to update the debug screen accordingly.

Again, nothing in the cited passage indicates that information comprising at least one internal state of the hardware model is "vital" to a co-simulation system. The cited passage describes a particular invention where internal registers and status of a device are available to a user to provide debug control. Nothing in this passage indicates that such is necessary or vital for all co-simulation systems.

Accordingly, Applicants traverse the Examiner's official notice and respectfully request that the Examiner provide a reference or references that disclose that information comprising at least one internal state of the hardware model would be vital to any hardware-software co-simulation system. Second, with respect inherency, the Federal Circuit has stated:

> To serve as an anticipation when the reference is silent about the asserted inherent characteristic, such gap in the reference may be filled with recourse to extrinsic evidence. Such evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference and that it would be so recognized by persons of ordinary skill.

Continental Can Co. USA v. Monsanto Co., 20 USPQ2d 1746, 1749-50 (Fed. Cir. 1991). Since the evidence provided by the Examiner does not show that information comprising at least one internal state of the hardware model is vital or otherwise necessary to a hardware-software co-simulation system, there is no evidence that such disclosure is necessarily present in Bhandari. Thus, Bhandari does not inherently teach the aforementioned feature.

The Examiner also stated that Klein teaches a shared memory for holding first information of a software model and second information of a hardware model, where the software model is capable of directly accessing the second information of the hardware model. (Office Action, pp. 7-8). The Examiner concluded that it would have been obvious to apply the teachings of Klein in the system of Bhandari. (Office Action, p. 8). Applicants respectfully disagree.

Klein discloses co-simulation of a hardware-software system design. (See Klein, Abstract). The software portion of the design is simulated using an instruction set simulator (ISS). The hardware portion of the design is simulated using a logic simulator in conjunction with software-based processor and memory models. (Klein, col. 5, lines 6-65; FIG. 2). Both the logic simulator and the ISS are software-based simulators. (Klein, col. 5, lines 43-50; col. 2, lines 6-8). The software described in Klein performs the hardware and software simulations with a single coherent view of the memory of the hardware-software system being co-simulated. (Klein, col. 4, lines 15-21).

The cited references, either singly or in any permissible combination, do not teach, suggest, or otherwise render obvious Applicants' invention recited in claim 1. Namely, the combination of Bhandari and Klein does not teach or suggest a "shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Klein discloses a complete software simulation system that simulates software and hardware portions of a circuit design. Klein does not teach or suggest simulating the hardware portion of the design in hardware using an emulator or other type of reconfigurable hardware. Thus, Klein cannot add anything to Bhandari with respect to the modeling of hardware using the external hardware systems, as the software modeling of hardware is

different than modeling hardware using a hardware device.

Moreover, the "single coherent view of memory" in Klein is not a physical shared memory, as recited in Applicants' claim 1. Rather, it is a logical construct of a memory portion of the hardware-software design being co-simulated. Moreover, the "memory" referred to in Klein is not the memory of the co-simulation system, but is rather the memory portion of the design being co-simulated. This logical memory construct described in Klein does not add anything to the communication of physical signals between the simulator and the external systems in Bhandari.

Accordingly, Klein does not bridge the substantial gap between Bhandari and Applicants' invention recited in claim 1. Namely, Klein does not provide a teaching or suggestion of a shared memory as recited in Applicants' claim 1 that can be incorporated into or otherwise modify the system of Bhandari to arrive at the invention of Applicants' claim 1. Therefore, Applicants contend that no conceivable combination of Bhandari and Klein renders obvious Applicants' invention of claim 1.

Independent claims 19, 24, 30, 33, 38, and 44 each recite features similar to those of claim 1 emphasized above. For the same reasons discussed above, Applicants contend that no conceivable combination of Bhandari and Klein renders obvious Applicants' invention of claims 19, 24, 30, 33, 38, and 44. Claims 2-6, 20-23, 25-29, 31-32, 34-36, and 45-46 depend from claims 1, 19, 24, 30, 33, 38, and 44 and recite additional features therefor. Since the cited combination does not render obvious Applicants' invention recited in claims 1, 19, 24, 30, 33, 38, and 44, claims 2-6, 20-23, 25-29, 31-32, 34-36, and 45-46 are also nonobvious. Accordingly, Applicants contend that claims 1-6, 19-36, 38, and 44-46 are patentable over the cited references and, as such, fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

B. Claims 7 and 10

The Examiner rejected claims 7 and 10 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein and further in view of RO'1998. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari and Klein into the instant section. Applicants submit that Bhandari or Klein, alone or in combination to not render dependent claims 7 and 10 obvious, at least for their dependency upon independent claim 1 (see above). The addition of RO'1998 does not correct the shortcomings of Bhandari and/or Klein.

For example, RO'1988 teaches Q-modules without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, and/or RO'1998 do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claim 1. Therefore, dependent claims 7 and 10, which depend either directly or indirectly from claim 1, are nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

C. Claims 8-9 and 11-18

The Examiner rejected claims 8-9 and 11-18 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of RO'1998, further in view of VA'1997. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari, Klein, and of RO'1998 into the instant section. Applicants submit that Bhandari, Klein, and/or RO'1998, alone or in combination, do not render obvious dependent claims 8, 9, and 11-18, at least for their dependency upon independent claim 1 (see above). The addition of VA'1997 does not correct the shortcomings of Bhandari, Klein, and/or RO'1998.

For example, VA'1997 teaches delay insensitive modules without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, RO'1998, and/or VA'1997, do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claim 1. Therefore, dependent claims 8, 9, and 11-18, which depend either directly or indirectly from claim 1, are nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

D. Claim 37

The Examiner rejected claim 37 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, and further in view of Butts. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari, and Klein into the instant section. Applicants submit that Bhandari or Klein, alone or in combination do not render obvious dependent claim 37, at least for its dependency upon independent claim 33 (see above). The addition of Butts does not correct the shortcomings of that Bhandari and/or Klein.

Butts teaches interconnected FPGAs without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, and/or Butts, do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claim 33. Therefore, dependent claim 37, which depends from claim 33, is nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of claim 37 be withdrawn.

E. Claims 39-43 and 47-50

The Examiner rejected claims 39-43 and 47-50 under 35 U.S.C. §103(a) as being unpatentable over Bhandari in view of Klein, further in view of BI'1997. Applicants traverse the rejection.

Applicants incorporate the arguments presented above with respect to Bhandari, and Klein into the instant section. Applicants submit that Bhandari or Klein, alone or in combination do not render obvious dependent claims 39-43 and 47-50, at least for their dependency upon independent claims 38 and 44 (see above). The addition of BI'1997 does not correct the shortcomings of that Bhandari and/or Klein.

BI'1997 teaches hardware/software co-simulation without any teaching or suggestion of "shared memory for storing information from both a hardware model and a software shared memory for holding a first information of a software model and a second information of the hardware model, where the software model is capable of directly accessing the second information of the hardware model." Since Bhandari, Klein, and/or BI'1997, do not teach or suggest these features, no conceivable combination of these references can teach or suggest Applicants' invention of claims 38 and 44. Therefore, dependent claims 39-43 and 47-50, which depend from claims 38 and 44, are nonobvious in view of the cited references and fully satisfy the requirements of 35 U.S.C. §103. Applicants respectfully request that the rejection of such claims be withdrawn.

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CONCLUSION

Thus, Applicants submit that all claims now pending are in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issuance are earnestly solicited.

If, however, the Examiner believes that any unresolved issues still exist, it is requested that the Examiner telephone Mr. Robert M. Brush at (732) 935-7100 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

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